

# Peers' evaluation of a reconfigurable IEEE1451.0-compliant and FPGA-based weblab

Ricardo J. Costa<sup>1,2</sup>, Gustavo R. Alves<sup>1</sup>, Mário Zenha-Rela<sup>2</sup>,  
Danilo Garbi Zutin<sup>3</sup>, Johan Zackrisson<sup>4</sup>, Willian Rochadel<sup>5</sup>, Unai Hernández-Jayo<sup>6</sup>

ISEP/CIETI/LABORIS<sup>1</sup>, FCTUC/CISUC<sup>2</sup>, CUAS<sup>3</sup>, BTH<sup>4</sup>, UFSC<sup>5</sup>, UD<sup>6</sup>

[rjc@isep.ipp.pt](mailto:rjc@isep.ipp.pt); [gca@isep.ipp.pt](mailto:gca@isep.ipp.pt); [mzrela@dei.uc.pt](mailto:mzrela@dei.uc.pt);

[d.garbizutin@fh-kaernten.at](mailto:d.garbizutin@fh-kaernten.at), [johan.zackrisson@bth.se](mailto:johan.zackrisson@bth.se), [willian.rochadel@ufsc.br](mailto:willian.rochadel@ufsc.br), [unai.hernandez@deusto.es](mailto:unai.hernandez@deusto.es)

**Abstract** – It is already more than 10 years that weblabs are seen as important resources to provide the experimental work required in engineering education. Several weblabs have been applied in engineering courses, but there are still unsolved problems related to the development of their infrastructures. For solving some of those problems, it was implemented a weblab with a reconfigurable infrastructure compliant with the IEEE1451.0 Std. and supported by Field Programmable Gate Array (FPGA) technology. This paper presents the referred weblab, and provides and analyses a set of researchers' opinions about the implemented infrastructure, and the adopted methodology for the conduction of real experiments.

**Keywords** - Weblabs, Remote labs, Remote experimentation, IEEE1451.0 Std., validation, verification.

## I. INTRODUCTION

Currently, weblabs are seen as important resources for engineering education [1][2]. However, the lack of standardization for their development and access, encouraged the implementation of an infrastructure compliant with the IEEE1451.0 Std. [3] that describes the so-called smart transducers and the way these can be network-interfaced. To provide the same facilities of traditional laboratories, where users (students and teachers) can setup experiments by selecting different instruments, it was also decided to provide a reconfiguration capability to the weblab infrastructure, taking the advantage of the reconfiguration nature of FPGAs that enable embedding hardware circuits in their cores. The involved research and developments of the implemented weblab was already presented by the authors through several publications [4][5][6]. The focus of this paper is the validation & verification process of the implemented architecture and underlying infrastructure, according to several researchers' opinions involved in the development of weblabs.

Section II of this paper provides an overview of the architecture and underlying infrastructure. Section III presents the objectives and the strategy followed in the validation & verification process. Section IV describes the selected experiments, and section V the implemented methodology. Before conclusions, section VI presents and analyses the opinions reported by the researchers.

## II. IMPLEMENTED WEBLAB ARCHITECTURE AND THE UNDERLYING INFRASTRUCTURE

The weblab infrastructure is part of an architecture that supports the selection, reconfiguration and standard access to different weblab modules used to control and monitor a specific experiment. These weblab modules (e.g. oscilloscopes, multimeters, switches, or others) are able to be remotely bond to the infrastructure in the same way students and teachers may select a specific instrument in a traditional laboratory to attach to an Experiment Under Test (EUT). Furthermore, those modules are accessed using standard commands provided by the IEEE1451.0 Std. HTTP API, and they can be easily replicated and embedded, through a reconfiguration process, into the weblab infrastructure.

As represented in figure 1, the weblab architecture comprises an underlying infrastructure and a Weblab Server. The infrastructure was designed according to the reference model of the IEEE1451.0 Std.. It integrates a Network Capable Application Processor (NCAP), implemented by a micro web server connected to a Transducer Interface Module (TIM), this implemented by an FPGA-based board. The NCAP provides the IEEE1451.0 HTTP API that enables the remote access to the TIM, which internally embed an IEEE1451.0-compliant module bonding the weblab modules through Transducers Channels (TCs). These modules are described through hardware description files and their features are defined using one or more Transducers Electronic Data Sheets (TEDSs), as defined by the IEEE1451.0 Std..

There are two distinct connections between the NCAP and the TIM. The first is the access connection used to control the operation of the weblab modules. The second is a reconfiguration connection that allows reconfiguring the TIM for bonding those weblab modules. The remote control is made by a direct access to the NCAP using the API, while the reconfiguration requires the use of a Reconfiguration Tool (RecTool) provided by the Weblab Server. This RecTool, whose part of the interface is illustrated in figure 2, is accessible through the web. It allows remote users to upload files defining the weblab modules, and configuration files containing all the instructions required to redefine the IEEE1451.0-compliant module so it can bond those modules.