

Work-in-progress on a thin IEEE1451.0-architecture to implement reconfigurable weblab infrastructures

Ricardo J. Costa^{1,2}, Gustavo R. Alves¹, Mário Zenha-Rela²
ISEP/CIET/LABORIS¹, FCTUC/CISUC²
rjc@isep.ipp.pt; gca@isep.ipp.pt; mzrela@dei.uc.pt

Abstract- Institutions have been creating their own specific weblab infrastructures. Usually, they use distinct software and hardware architectures comprehending instruments and modules (I&M) able to be parameterized but difficult to be shared. These aspects are impairing their widespread in education, since collaboration between institutions, in developing and sharing resources, is still low. To handle both aspects, this paper proposes the adoption of the IEEE1451.0 Std. with FPGA technology for creating reconfigurable weblab infrastructures. It is suggested the adoption of an IEEE1451.0 infrastructure with compatible instruments, described in Hardware Description Languages (HDL), to be reconfigured in FPGA-based boards. Besides an overview of the IEEE1451.0 Std., this paper presents a solution currently under development which seeks to enable the reconfiguration and the remote control of weblab infrastructures using a set of IEEE1451.0 HTTP commands.

Keywords: *Weblabs, Remote laboratories, IEEE1451.0 Std., Reconfiguration, FPGAs.*

I. INTRODUCTION

Typical classrooms are being complemented and, in some cases, replaced by new technology-based tools. This is obvious in faculties, justified by the appearance of the internet and associated services that give students easy access to several educational contents and teachers the adoption of web tools to facilitate the teaching/learning processes. Weblabs are examples of technological appliance in education that allow the access to real laboratories using a device connected to the internet (e.g. a PC) for conducting experiments. Currently, many institutions are applying them in their courses, some available through the library of labs portal [1]. However, there is still a lack of standardization in weblab infrastructures, difficulting the development and the share of resources. These aspects impair institutional collaboration, since the adopted I&M do not use standardized interfaces, despite some proposals both at software and hardware levels [2][3][4][5][6][7]. Furthermore, typical weblab infrastructures use different platforms based on computers and independent instruments, increasing costs and contributing for low reconfiguration capabilities.

It is precisely in this scenario, characterized by current limitations, that the IEEE1451.0 Std. and FPGA technology are seen as possible solutions to create reconfigurable weblab infrastructures. The supporting facts are: the IEEE1451.0 Std. describes hardware and software layers to control and

network-interface transducers (which can also form the I&M used in weblabs), and FPGAs can be easily reconfigured with different embedded IEEE1451.0-compatible instruments described in standard HDL.

In this paper, section II briefly presents the main issues of the IEEE1451.0 Std.. Section III points recent applications of the standard, and justifies its adoption together with FPGAs for creating reconfigurable weblab infrastructures, referring previous work made by the authors. Section IV presents the work under development. It describes the implementation of a generic IEEE1451.0 infrastructure in an FPGA (currently interfacing two digital I/O modules), and some guidelines for future developments. Section V concludes the paper.

II. IEEE1451.0 STD. OVERVIEW

The IEEE1451.0 Std. [8] aims to network-interface transducers (sensors and actuators) and defines a set of operating modes, based on specifications provided by Transducer Electronic Data Sheets (TEDS). Defined in 2007, this standard is the basis for forthcoming and previous members of the IEEE1451.x family so they can operate together. The operating modes defined by the standard are controlled using low-level commands that can be applied using a set of APIs.

The standard defines an architecture based on two modules that should be interconnected using an interface protocol: the Transducer Interface Module (TIM) and the Network Capable Application Processor (NCAP). Each module is connected through an interface defined by another standard of the IEEE1451.x family, some already specified according to the IEEE1451.0 Std. (e.g. the IEEEp1451.6 Std. for the CANopen interface) and others intended to be modified in the future (e.g. IEEE1451.2 Std. which defines point-to-point interface). Figure 1 illustrates the IEEE1451.0 Std. main modules, and associated layers.

Each TIM may contain up to 32767 (2^{15}) Transducer Channels (TC), controlled individually or in groups when they simultaneously control/monitor a specific physical phenomenon or transducer. The TIM and TC behaviors are specified by different TEDS and follow two operation state diagrams and two trigger state diagrams, one for sensors and another for actuators. Each state represents a transducer operating/trigger state that changes according to the defined operation mode. TEDS are implemented in 8 bit (octet) words inside the TIM, or can be remotely located (named virtual