ISEP-DEE Mestrado em Engenharia Electrotécnica e de Computadores

Tese/Dissertação (Proposta)

Ano lectivo 2011/12

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NPGA: Network-Programmable Gate-Array

Nome do Aluno:

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Breve descrição do trabalho:

With the continuation of Moore's law, it is expected that in the near future, it will be possible to deploy computer networks comprising a very large number of computer nodes, where each computer node has sensing and wireless communication capability and those computer nodes can collaboratively obtain/estimate the state of the physical environment. For example, such computer network can (i) find out how to cancel noise, (ii) decide if a human being is present in a room or (iii) decide if a senior person has fallen from bed.

The large number of computer nodes generates an enormous amount of sensor readings. But applications are only interested in a few sensor readings or an aggregated quantity of those. This poses the important challenge of how to combine sensor readings to produce useful aggregated quantities and to do it efficiently. Given the large scale and dense nature of those systems, it is imperative that the time complexity does not depend on the number of nodes.

Recent research at the CISTER Research Unit at ISEP has produced an algorithm, based on detecting an unmodulated carrier wave, that makes it possible to compute MIN/MAX of sensor readings with a time-complexity that is independent of the number of computer nodes. With this approach, it is also possible to compute the logical functions AND, OR, NAND and NOR. Since it is known that any logical function can be decomposed into NAND-functions, it is interesting to explore how a logical function should be decomposed in order to

take advantage of the efficient approach for computing NAND which performs

based on detecting an unmodulated carrier wave.

The goal of this project is therefore to explore how to implement logical functions (for example described with VHDL) on computer nodes using the approach of detecting an unmodulated carrier wave.

The required technology is available at the CISTER Research unit (see: http://www.hurray.isep.ipp.pt/activities/PRIOMAC)

Outros dados relevantes:

Por favor enviar e-mail com CV resumido para mjf@isep.ipp.pt

Para mais informações sobre as actividades de I&D do CISTER na área de redes de sensores, visite http://www.cister.isep.ipp.pt/research/sensor+networks/

Recursos necessários no DEE:

A Unidade de Investigação CISTER disponibilizará os equipamentos necessários. Em princípio, não serão necessários recursos do DEE, a não ser apoio no desenvolvimento de potenciais plataformas de hardware.

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