# Gatewaying IEEE 1149.1 and IEEE 1149.7 Test Access Ports

Francisco R. Fernandes, Ricardo J. S. Machado, José M. Ferreira
Department of Electrical and Computer Engineering
FEUP
Porto, Portugal
{francisco.fernandes, machado.ricardo, jmf}@fe.up.pt

Manuel G. Gericota
Department of Electrical Engineering
ISEP
Porto, Portugal
mgg@isep.ipp.pt

***Abstract*— In this paper, we present a description of our developed adapter, which takes acts as a gateway between IEEE 1149.1 and IEEE 1149.7 test infrastructures. The referred adapter reduces the pins of the TAP from 4 to 2 and implements advanced capabilities, such as Parking State of a TAPC and the Reset and Selection Unit (RSU).**

***Keywords- Boundary-scan; IEEE Std 1149.1; IEEE Std 1149.7; TAP;***

## I. INTRODUCTION

The boundary-scan test technology was developed in the mid-1980s and approved as IEEE Std 1149.1 in 1990 [1]. Every 1149.1-compliant circuit includes a set of test cells placed in the device boundary, enabling observation and control of every functional pin. The four-pin Test Access Port (TAP) ensures the access to the test infrastructure using a common protocol to all test data operations irrespective of the device or its manufacturer. There are two pins dedicated to data shifting (TDI and TDO), one pin dedicated to control operations (TMS), and one to provide the test clock (TCK). Each device possesses an instruction register (IR) which specifies the required operating mode for the test logic.

The IEEE Std 1149.7 [2] [3] maintains the compatibility with the previous standard, but it offers the possibility of not only to reduce the number of pins used for testing and debugging, while offering new and improved functionalities and topologies. This new standard, while fully compatible with the IEEE 1149.1, is not meant to replace it.

This standard enables the use of either the legacy TAP or a compact version using only 2 pins (TCKC and TMSC). It also offers the possibility of using a star topology of the test circuit, allowing the test of different circuits at the same time. It also provides new features like the chip-level bypass (where chains that are not used are substituted by a bypass bit), the individual addressing (allowing the communication exclusively with any given device) and the power management capabilities (to control the power consumption).

The main contribution of the work described in this paper is related to the integration of IEEE Std 1149.1 test systems and architectures in IEEE std 1149.7-based environments by the development and implementation of suitable adapters. Since the recent standard is only compatible with the legacy standard in some restricted architectures, a set of three scan format adapters were developed, in order to fully integrate the legacy standard test architecture in modern star topologies using 2 signals. The use of such adapters is useful to preserve IP cores that use a four wire test bus, on a chip that only uses two external pads. Also, the RSU module allows the control of the legacy TAPC, providing the capability to switch-on or switch-off the respective scan path.

## II. SCAN FORMATS

To meet the demands for improved capabilities and higher performance of the debug and test phase, 13 advanced scan formats are defined in the IEEE Std 1149.7. These advanced scan formats are only usable with classes T4 and T5 of the TAP.7, since these are the classes that provide advanced capability. Therefore, the behavior of the TAP.7, with these scan formats, is compatible only with Star-2 Scan Topology. Although having 13 advanced scan formats, only 3 are considered to be mandatory – MScan, OScan0 and OScan1. Each TCKC period represents a different test signal in the TMSC packet. Each of the mandatory scan formats have a different sequence of multiplexed data, as shown in figure 1.

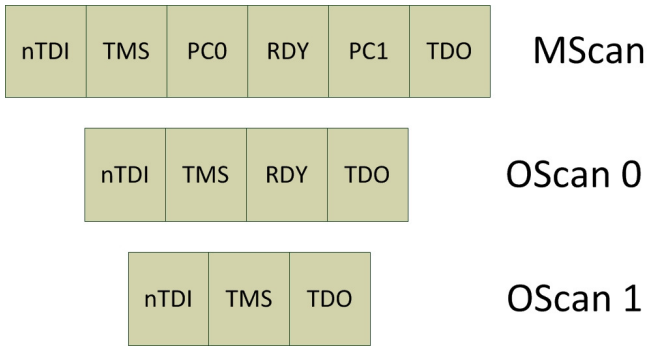


Figure 1. TMSC multiplexed data in MScan format

The PC0 and PC1 are precharge bits that occur before and after the RDY bits, respectively. The RDY vector may be used to stall the TAPC progression, which delays the completion of the transmission, until a ready sequence is detected.

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## III. EXTENDED FEATURES

Since the current circuits are increasing in complexity, the structure of the test architecture of the IEEE std 1149.7 is divided in multiple levels, in contrast to the legacy standard. The new standard has the possibility of creating an unlimited number of levels, divided in three classes: ADTAPCs (adapter TAPC); CLTAPCs (Chip-Level TAPC); EMTAPCs (Embedded TAPC). A TAPC is considered a parent of another TAPC when it is in a higher architectural level.

### *A. Parking States*

A TAPC is considered parked when the state of its parent may change, while its state does not change. This means that its state is no longer synchronized with the TAPs at higher levels of the hierarchy. One use of this feature is to disable the access to scan paths that are of no interest or are not available for use. An ADTAPC may be parked in any TAPC state. CLTAPCs may be parked in Test-Logic-Reset, Run-Test/Idle, Pause-IR and Pause-DR states, since they are stable states in the IEEE 1149.1 standard. An EMTAPC may only be parked in Test-Logic-Reset or Run-Test/Idle states. When a CLTAPC or an EMTAPC is parked in a forbidden state, an asynchronous TAPC reset is required to unpark it.

### *B. RSU Module*

When the selection and deselection of a T0 TAP.7 is desired, the optional RSU is placed between the TAP signals and the Chip-Level Logic. Figure 2 demonstrates the connectivity between the T0 TAPC and the RSU module.

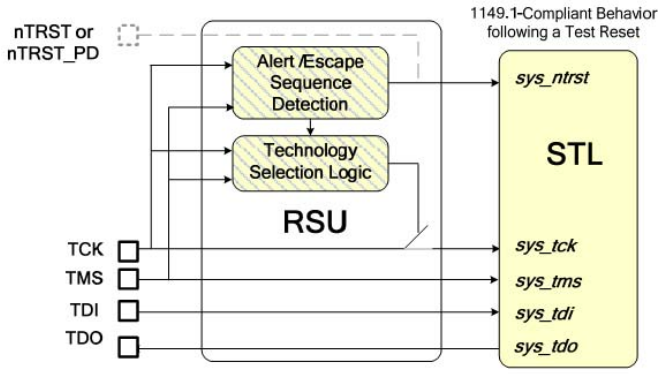


Figure 2. RSU and T0 TAP functional block diagram [2]

The RSU contains reset and selection/deselection capability. It supports the parking of the TAPC state. The actions taken by the RSU are initiated with Selection Alert Bit Sequences and Deselection Alert Bit-Sequences. The selection and deselection sequences are initiated by the DTS holding the system test clock high, and repeatedly changing the value of TMS. This indicates the RSU module that a selection or deselection sequence is arriving next, and consists of 4 bits called the OAC (Online Activation Code) field. If the OAC received matches the predetermined code of the RSU module, the respective Scan Path is either switched on or off, depending on the current state.

## IV. RESULTS

The three scan format adapters were implemented using the Xilinx® ISE Design Suite 13.3 and the Verilog HDL. An Xilinx® Spartan3 FPGA was used as the target device.

The adapter is the higher level module, and converts the data from two to four pins. The four test signals are then connected to the 1149.1 TAPC and the boundary scan chain. This allows a good analysis of resource allocation. All the implementations have different state machines, yet they all have a common initial stage: synchronization. At power up, the adaptor is unable to guess the phase of the multiplexed data signal. After synchronization each adaptor stores the multiplexed data in the respective registers in order to convert each packet into the four-wire communication protocol.

The RSU module was implemented using the OScan1 format. It consists of a module that is placed between the adapter and the TAPC modules, allowing a complete analysis of the incoming test signals and control of the TAPC.

Table I compares the resource utilization of each of the implementations described.

TABLE I. IMPLEMENTATION RESULTS

| Logic Utilization | MScan Adapter | OScan0 Adapter | OScan1 Adapter | OScan1 Adapter + RSU |
|---|---|---|---|---|
| Registers | 92 | 86 | 86 | 102 |
| 4 input LUTs | 89 | 88 | 86 | 80 |
| Slices | 79 | 75 | 74 | 78 |

## V. CONCLUSIONS AND FUTURE WORK

Analyzing the implementation results it is possible to infer the resources required by the adaptors and RSU module, compare those resources to assess the advantages of using only two pins dedicated for testing, and the possibility to select and deselect the TAPC individually or in groups. By using one of the three adapters it is possible to use an IEEE std 1149.1 component in a IEEE std 1149.7 star-2 architecture introducing the functionalities of the newer standard.

It is our goal to sequentially develop the remaining modules in the TAP.7 architecture, the Extended Protocol Unit (EPU) and Advanced Protocol Unit (APU). The development of adapters to the optional scan formats is also an objective.

## REFERENCES

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[3] A.W. Ley, "Doing more with less - An IEEE 1149.7 embedded tutorial: Standard for reduced-pin and enhanced-functionality test access port and boundary-scan architecture", International Test Conference, 2009. ITC 2009, 1-6 Nov. 2009