Using test infrastructures for (remote) online evaluation of the sensitivity to SEUs of FPGAs

André V. Fidalgo, Gustavo R. Alves, Manuel C. Felgueiras, and Manuel G. Gericota

LABORIS/ISEP

{anf, gca, mcf, mgg}@isep.ipp.pt

SRAM-based Field Programmable Gate Arrays (FPGAs) endured a considerable evolution in the last few years, both in terms of density and complexity, with nanometre technology being currently used in their manufacturing. However, the exponential growth of the number of memory cells needed for configuration purposes makes them especially vulnerable to radiation induced faults, like Single Event Upsets (SEU), even at ground level [1-3]. These faults can permanently degrade the performance or change the functionality of the circuit implemented on the FPGA in different ways, namely: (1) by changing the routing configuration; by modifying the contents of the (2) Look-Up Tables (LUT) or (3) dedicated memory blocks; and (4) by inverting the contents of the flip-flops located at the Configurable Logic Blocks (CLB) and the Input/Output (I/O) blocks. At this point we should distinguish between resources that are being (A) used and (B) not used. We propose an online mechanism capable of detecting all possible bit-flips in some of the resources not being used, namely 1B, 2B, and 3B parts, and also on some of those being used, namely 1A, as this information is static after the FPGA configuration process. Any bit-flip on an FPGA flip-flop, i.e. 4A and 4B parts will not be detected through the configuration memory. The information contained in the LUTs and dedicated memory blocks in use can be static or dynamic depending of the circuit implementation and functionality. Bit-flips occurring in 2A-static and 3A-static parts can also be detected depending on the architecture of the FPGA under evaluation. For instance, in FPGAs from the Virtex-II family, the contents of the configuration memory are accessed on a frame-per-frame basis. If a frame contains elements pertaining to 2A-dynamic and 3A-dynamic parts then this frame should not be read so as to avoid corrupting the contents of such dynamic parts [4]. This implies not being able to access the bit contents of all the other static parts addressable through that very same frame. Information about the FPGA configuration memory organization is usually provided by the manufacturer or, in its absence, it is still possible to extract structural information using methods reported in literature [5].

The online detection mechanism requires: a read value, an expected value, and a mask. In a usual FPGA + external configuration memory circuit the read value is a bit read from the FPGA internal configuration memory, irrespectively of the addressing method, the expected value is a bit read from the external configuration memory, and the mask is provided by architectural information related to the FPGA internal memory organization.

The detection circuit can be implemented in different ways depending on:

- Its location, i.e. if it will be configured into the FPGA (as a functional block) or if it will be external, thus only requiring a JTAG-compatible infrastructure to access the FPGA + external configuration memory.
- An external memory is required for the masks;
- The external configuration memory (and the previously referred one) is (are) JTAG-compatible.

The online detection mechanism will cyclically read and compare the values from the external and internal configurations memories, taking into account the mask information, and signal any mismatch as a result of a SEU affecting both used and not-used FPGA parts, which maximises the monitored area. Using an external, web-accessible controller, connected to the test infrastructure, enables the possibility to run the same operations in a remote fashion, with the additional benefit of eliminating the need for a local memory storing the mask values.

References

[1] R. Velazco, F.J. Franco, "Single Event Effects on Digital Integrated Circuits: Origins and Mitigation Techniques," Proc. IEEE Intl. Symposium on Industrial Electronics, pp.3322-3327, 2007.

[2] M. Bellato, P. Bernardi, D. Bortolato, A. Candelori, M. Ceschia, A. Paccagnella, M. Rebaudengo, M. S. Reorda, M. Violante, P. Zambolin, "Evaluating the effects of SEUs affecting the configuration memory of an SRAM-based FPGA", *Proc. of the DATE Conf.*, pp. 584-589, 2004.

[3] H. Quinn, P. Graham, J. Krone, M. Caffrey, S. Rezgui, C. Carmichael, "Radiation-Induced Multi-Bit Upsets in Xilinx SRAM-Based FPGAs", *Proc. Military and Aerospace Appl. of Prog. Logic Devices Conf.*, 2005.

[4] Bridgford, B., Carmichael, C., W. Tseng, C., "Correcting Single-Event Upsets in Virtex-II Platform FPGA Configuration Memory", *Xilinx Application Note XAPP779 (v1.1),* February 2007.

[5] J.-B. Note, E. Rannaud, "From the bitstream to the netlist," Proc. 16th Intl. ACM/SIGDA Symp. on FPGAs, pp. 264, 2008.

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