IEEE Std 1149.7: What? Why? Where?

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Abstract — **The IEEE Std 1149.7 holds the promise of great improvements for testing electronic circuits, when used along with other IEEE standards (particularly those that use the IEEE Std 1149.1 for test access and control). In this paper we describe "what" is the IEEE Std 1149.7, the reasons "why" we may consider to use it instead of IEEE Std 1149.1, and we highlight the application spectrum "where" this new standard can be useful.**

Keywords – Boundary-scan; IEEE Std 1149.1; IEEE Std 1149.4; IEEE Std 1149.6; IEEE Std 1149.7; IEEE Std 1500; IEEE Std 1532; IEEE Std 1581; IEEE P1687; IEEE P1838; Nexus 5001; TAP; JTAG; iJTAG;

I. INTRODUCTION

Several technological improvements that took place over the years enabled the development of highly complex Integrated Circuits (ICs) using Intellectual Property (IP) cores that greatly reduce the time-to-market for complex devices. The need and opportunity for the development of Systems-on-Chip (SoC) also led to a significant increase in the difficulty of testing, verification and debugging. One of the main issues is that automated SoC testing is only possible if further developments take place in testing standards, widening their scope and enhancing their controllability, observability and speed. Therefore, components are increasingly required to support integrated standard test infrastructures.

The boundary-scan test technology (also known as JTAG) started to be developed in the mid-1980s and was approved as IEEE Std 1149.1 in 1990 [1]. Every 1149.1-compliant circuit includes a set of test cells placed in the device boundary, enabling observation and control of every functional pin. The four-pin Test Access Port (TAP) ensures access to the test infrastructure using a common protocol to all test functions, irrespective of the device or its manufacturer. There are two pins dedicated to data shifting (TDI and TDO to shift in / out), one pin dedicated to control operations (TMS to select the required test mode), and another one to provide the test clock (TCK). Each device possesses an instruction register (IR), present in the same scan chain, which specifies the required operating mode for the test logic. The miniaturization of the fabrication processes and the much higher integration densities led to smaller chips that are strongly pin-bounded, while at the same time enabling a reduction of the production cost of the chip. However, the new fabrication techniques reinforced the emergence of new types of physical defects such as latch-up, electrostatic discharges, electromigration and hot-carrier degradation [2] [3]. All these factors contributed to the appearance of a new test standard: IEEE Std 1149.7 [4] [5]. This new standard maintains the compatibility with its predecessors, while offering the possibility of reducing the number of pins used for debug and test (D&T), and adding new and improved functionalities.

This paper offers a brief description of the IEEE Std 1149.7, discusses the added value of the new features offered to designers and test engineers, and highlights how this new standard can positively impact its predecessors.

The paper is organized as follows. Section II provides an insight on the new IEEE Std 1149.7 ("What?"). Section III focuses on the new features and their added value ("Why?"). Section IV briefly looks at the intersection of the IEEE Std 1149.7 with several other competing or complementary standards ("Where?"). Section V closes the paper.

II. WHAT?

Ratified in December 2009 and published in February 2010, the IEEE Std 1149.7 is the most recent of the IEEE Std 1149.X standards and aims at improving the test of digital electronic circuits. The IEEE Std 1149.7, formally named *IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture*, is a superset of the IEEE Std 1149.1. While fully compatible with the IEEE Std 1149.1, this new standard is not meant to replace it.

The main objective of IEEE Std 1149.7 is to cope with the new challenges of debug and test systems (DTS), while protecting the investments made by manufacturers that have been using the IEEE Std 1149.1. These new challenges can be at D&T level or at functional level, namely the need for better performance when a TAP is used for debugging, the possibility of transmitting data through the test structure, the control of several chips using a single TAP Controller (TAPC), and the control of several TAPC using only one TAP. It also offers a solution to the need for reducing the number of pins and the power consumption levels.

In order to ensure the new features described above, while maintaining compatibility with the IEEE Std 1149.1, the TAPC of the IEEE Std 1149.7 is structured hierarchically. This structure consists of six types of operations (T0-T5) divided in three classes. The three classes of operations defined by this standard are: “Legacy”, which inherits IEEE Std 1149.1 operations; “Extended”, which supports new functionalities while continuing to use four test pins; and “Advanced”, where all the new functionalities are available using two or four test pins. Figure 1 shows the hierarchical structure of the IEEE Std 1149.7.

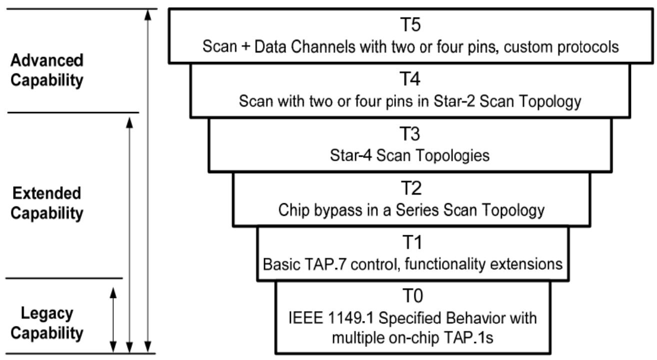

Figure 1. TAP.7 Capability Classes [2]

To reduce the power consumption, the new test structure can be completely powered-down. In order to face the challenges of managing several test structures from different chips at the same time, this new standard allows the connection of D&T systems in three ways: Four-wire Series Scan Topology, Four-wire Star Scan Topology, and Two-wire Star Scan Topology. The IEEE Std 1149.1 is only compatible with the Four-wire Series Scan Topology, and the other two are exclusive to IEEE Std 1149.7 compliant circuits. These three topologies are shown in figure 2.

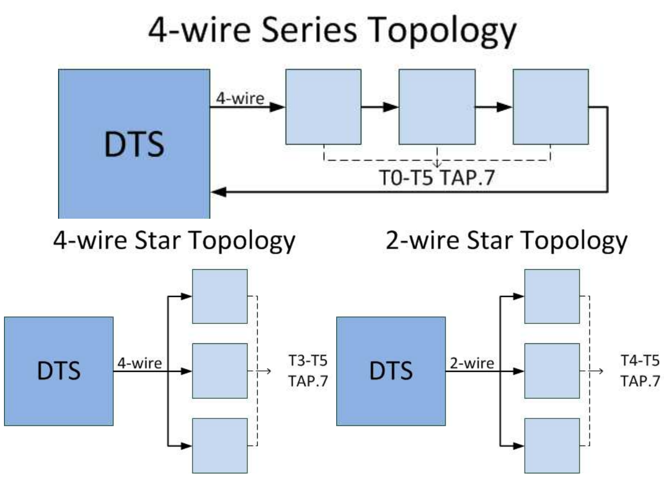

Figure 2. Series, Star-4 and Star-2 Scan Topologies

The majority of chips are currently pad-limited, meaning that their functionality is limited by the number of pins, not by the complexity of their internal circuitry. The possibility of using only two pins for testing instead of four should be determinant for the industry acceptance of this standard, as it lowers the cost of the manufacturing process, and at the same time widens the usefulness of the built-in test infrastructure.

The IEEE Std 1149.7 is not meant to replace the IEEE Std 1149.1. All the previous investments made to date in hardware, software IP and existing D&T tools can be preserved since the new standard is fully compatible when using the “Legacy” class of operation in the TAPC.

III. WHY?

The goal of this new standard is to improve the application domain of the IEEE std 1149.1 and to extend its capabilities in order to cope with the recent changes in integrated circuit technology and topology.

A. Reduced Pin Count

One of the most important features in the IEEE Std 1149.7 is the use of a 2-pin TAP, with D&T data transfer using only TCK and TMS, now renamed TCKC and TMSC. All data (TMS, TDI and TDO vectors) is multiplexed into the TMSC signal according to one of the supported scan formats. TDI and TDO can now be removed without affecting any of the previous functionalities or compromising the new extended or advanced protocols. This reduction in the number of pins is significant due to the severe size constraints of most modern embedded systems and general ICs. Dedicated pins for test and debug features are desirable during board development but raises the overall cost of the devices.

The IEEE Std 1149.7 enables access to further D&T functionalities using a smaller number of pins. Fewer pins, nets and discrete components such as pull-up resistors, also make routing and layout much easier, particularly in applications like stacked-die devices and multi-chip modules (2.5D and 3D chips), where several components are vertically stacked. Reducing the number of pins needed for test also lowers the overall packaging cost, releases pins for implementing additional features, and helps device and board designers to meet their cost constraints.

The supported scan formats (13 defined, 3 mandatory) have different multiplexing strategies according to the envisaged D&T functionality. These formats are optimized for boundary-scan, debug, control, or shifting data. Data that is not required can simply be skipped, improving D&T time, while reducing cost.

B. Star Topology

The star topology is one of several enhancements in the IEEE Std 1149.7 for handling arrays of identical devices and devices with multiple cores. Examples of such design scenarios are boards with multiple DSPs or multi-core CPU, or Systems-on-Chip (SoC) with separate physical processors, stacked die configurations, or multichip System-in-Package (SiP) modules with several distinct peripherals within the same physical package.

The introduction of a star topology in the IEEE Std 1149.7 complements the reduction in the number of test pins. Designers working with stacked-die devices, multi-chip modules and plug-in cards will favor the star topology and 2-pin interface because it simplifies the physical connections between devices.

C. Chip-level Bypass

The IEEE Std 1149.7 not only provides better support to devices with multiple cores and internal peripherals, but does so more efficiently. The serial design architecture of the IEEE Std 1149.1 made it difficult to communicate exclusively with one device due to unavoidable interactions with other devices in the same chain, particularly when multiple devices or cores are combined into one physical package. The new standard provides a method to address and access individual devices in the scan chain, without shifting bits through the entire instruction register scan chain, as seen in figure 3.

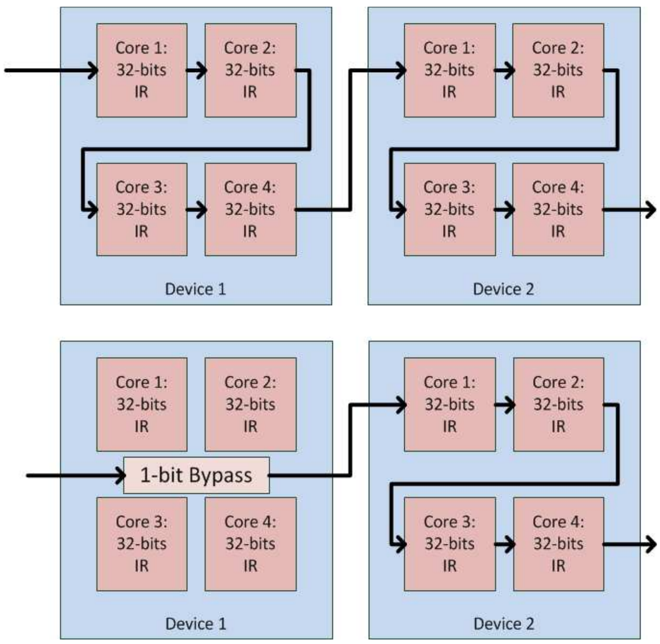

Figure 3. Scan path without and with Chip-level Bypass

A chip level bypass mechanism has been implemented to reduce the overall scan chain length by setting unused devices into a 1-bit chip bypass mode. This feature can make very long scan chains dramatically shorter, and improves the overall scan efficiency and throughput.

D. Individual Device Addressing

The individual addressing and chip level bypass capability provided by this new standard allows the host controller to communicate exclusively with any given device. This improves performance and facilitates the design of more advanced debug and instrumentation logic into individual chips, while enabling the host controller to address multiple internal modules through the same 2 or 4-pin TAP interface. The ability to quickly access a specific device in a system with multiple devices is also important to improve the debugging of complex systems. This is highly relevant because the International Technology Roadmap for Semiconductors (ITRS) currently expects that the number of internal cores will roughly double with each new processor generation [6].

E. Power Management

In the IEEE Std 1149.1 all devices have a two power state while being tested: It has to be either completely on or completely off while D&T operations are running. The IEEE Std 1149.7 provides a standard interface with four selectable power modes to control power consumption. The ability to adjust the power state of multiple cores in a device makes D&T much easier in many scenarios.

IV. WHERE?

Since the introduction of the IEEE Std 1149.1, several companies adopted it to meet their own challenges. On the other hand, the emergence of new application fields led to the development of new standards. This is the case of the closely related IEEE Stds 1149.4 [7] and 1149.6 [8], and the 1149.1-dependent IEEE Stds 1500 [9] [10], 1532 [11], 1581 [12] [13] [14], the IEEE proposals P1687 [15] and P1838 [16], and the Nexus 5001 standard [17]. While addressing different application fields, they all rely on the IEEE Std 1149.1, as shown in figure 4. Since the latest IEEE Std 1149.7 is a superset of IEEE Std 1149.1, it is itself related to all these standards. In fact, some of its new features are designed to face the challenges of the application areas of those standards. As such the IEEE Std 1149.7 deviates from the original application field of IEEE Std 1149.1, and introduces itself to "newer" areas, e.g. debugging, multi-chip or SoC D&T, die-stacked chips, chip programming, etc.

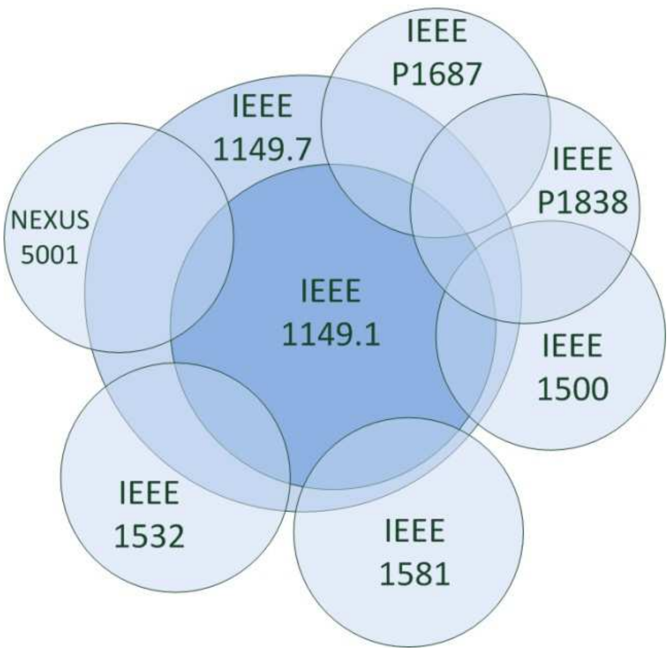

Figure 4. Relationship between IEEE standards

A. *IEEE Std 1149.4*

The IEEE Std 1149.4 [7] was developed to enable IEEE Std 1149.1 to cope with mixed signal electronic circuits. As such, some test blocks had to be changed or added to test the analog parts of the circuits: a two-pin Analog Test Port (ATAP), an internal analog test bus (with two lines), a Test Bus Interface Circuit (TBIC), and Analog Boundary Modules (ABMs).

Although this standard was designed to enable the test of analog circuits, its register structure was completely digital, and similar to the one used in the IEEE Std 1149.1. Silicon overhead and the effect of the ABMs in the highly sensitive analog signals prevented industry acceptance and this standard never made it to the market.

Due to the nature of mixed-signal circuits, the advantages that the new IEEE Std 1149.7 can provide are limited to the control structure, especially by using only two digital test pins. The power management of the test infrastructure can also be seen as a significant improvement.

B. *IEEE Std 1149.6*

The IEEE Std 1149.1 uses only static logic signals for test purposes. The IEEE Std 1149.6 [8] was developed to cope with high-speed digital networks that use differential or AC-coupled interconnections. This standard enabled high fault coverage of AC-coupled electronic circuits and devices that use Low Voltage Differential Signaling (LVDS), ensuring minimum impact on mission logic. One of its promises was to reuse as much as possible IEEE Std 1149.1 tools to guarantee backward compatibility.

Again, due to the nature of the 1149.6 application domain, the extended features of the IEEE Std 1149.7 have an impact mainly on the digital access and control structure, while adding power management features.

C. *IEEE Std 1500*

With the increasing complexity of integrated circuits (IC), the use of multiple embedded cores in one chip became common. Testing these components became a huge challenge for IC designers. A standard solution was proposed by the IEEE Std 1500 working group [9], with the main objective of developing a core-level approach to allow test integration and test reuse. This solution was based on combining a hardware architecture and an information model based on the Core Test Language (CTL).

The IEEE Std 1500 hardware architecture comprises a set of registers: the Wrapper Instruction Register (WIR), the Wrapper Bypass Register (WBY) and the Wrapper Boundary Register (WBR). The IEEE Std 1500 architecture also comprises a set of I/O signals, which constitute the Wrapper Interface Ports. There are two categories of ports: the Wrapper Serial Ports (WSP) and the Wrapper Parallel Ports (WPP). WSPs are used to load all the serial instructions and to communicate with the WIR and the WBY. In addition to WSPs, the IEEE Std 1500 also supports a parallel test access mechanism (TAM) called Wrapper Parallel Ports (WPPs). WPPs are optional ports that are used to increase the test bandwidth. These ports are used when the serial port cannot transfer the necessary amount of test data within a certain time interval. The WBR allows access to the core terminals through the wrapper ports, and comprises wrapper boundary cells (WBCs) that can simply be single storage devices (only for observation purposes), or cells with a certain complexity, comprising shift paths with multiple storage devices.

One of the innovative features of the IEEE Std 1500 is that it binds its hardware architecture to a specific test description language: the IEEE Std 1450.6 *Core Test Language* (CTL) [18], which is itself a subset of the IEEE Std 1450 - *Standard Test Information Language* (STIL). The CTL was developed with the objective of allowing specific design data description for testing integrated cores. One of the main achievements of the IEEE Std 1500, together with the CTL, is the possibility of automating test reuse, from the initial core design stage to the final core integration stage.

Both the IEEE Std 1149.1 and the IEEE Std 1500 improved the testing process, but their focus differs significantly. IEEE Std 1149.1 is primarily concerned with structural testing of digital printed circuit boards, and much less with internal IC testing. On the other hand, the IEEE Std 1500 is primarily concerned with embedded core testing and user defined logic within an IC. The IEEE Std 1500 architecture was designed to allow interface compatibility with the IEEE Std 1149.1 test access port (TAP) controller, and the wrapper's WSC interface matches the control outputs of the IEEE Std 1149.1 TAP controller.

Since the IEEE Std 1500 is fully compliant with the IEEE Std 1149.1, interoperability with the IEEE Std 1149.7 is guaranteed, with the additional possibility of using the extended features introduced by this new standard.

D. *IEEE Std 1532*

The IEEE Std 1532 [11] was developed by a group of experts from programmable logic vendors, the boundary-scan test industry and suppliers of in-circuit test systems. The mission of the group was to define, document, and promote the use of a standard process and methodology for configuring programmable devices using the IEEE Std 1149.1 communication protocol.

This standard enables one or more compliant devices to be programmed concurrently on a board or embedded in a system (improving efficiency through in-system configuration). This feature addresses the need to configure or reconfigure, read back, verify or erase programmable devices after being assembled. It avoids handling damage and minimizes manufacturing steps and inventory management costs.

The IEEE Std 1532 was adopted in 2001 and updated in 2002 to include a programming data file format and a method for implementing adaptive programming algorithms. The standard requires that devices comply with the IEEE Std 1149.1 for transmitting the data for programming, erasing, verifying, securing or other operations. The Boundary Scan Description Language (BSDL) is necessary to describe IEEE

Std 1532 and IEEE Std 1149.1 features. In addition, the IEEE Std 1532 defines a format for the programming data.

Since the IEEE Std 1532 uses the IEEE Std 1149.1 communication protocol, the impact of the introduction of IEEE Std 1149.7 is restricted to that area. The use of 2 pins and dedicated scan formats can improve the programming tasks, particularly because all data has to be transmitted serially. This means that the number of TCK cycles is equal to the sum of the selected registers length in all devices. With the IEEE Std 1149.7 star topology it is possible to program multiple (similar) devices, transmitting the program sequence only once. In the case of in-system configuration, the power management features can be useful when the programming stage is over.

E. IEEE Std 1581

The IEEE Std 1581 [12] defines a low-cost method for testing the interconnection of discrete, complex memory integrated circuits, where additional pins for testing are not available, and where a boundary scan infrastructure is not feasible. It specifies the implementation rules for test logic and test mode entry/exit methods. The IEEE Std 1581 is aimed at ICs that are otherwise not provisioned with design for testability (DfT), offering a solution to test their interconnections on PCBs. This is particularly important in the case of ball grid arrays (BGAs) and other highly compact packages, where prototype testing is much more complex. The complementary features of IEEE Std 1581 and IEEE Std 1149.1 simplify the testing of memory-based circuits, which are frequently limited to basic bridging and stuck-at faults. However, open circuit defects (which are the majority of soldering defects) are still not detectable.

While IEEE Std 1149.1 provides an efficient mechanism for reading and writing test patterns to a memory conformant to IEEE Std 1581, this standard does not forbid other access means for testing purposes. The Control Device, which is IEEE Std 1149.1 compliant, is responsible for generating the test stimuli to be applied to the IEEE Std 1581 device through the Input Bus, and also to capture the responses generated by the internal test logic via the Output Bus. According to the IEEE Std 1581, there are two ways of entering/exiting the test mode: the use of a dedicated test pin (TPN) or through the so-called transparent test mode (TTM). The first possibility uses a dedicated Test Pin (TPN), that forces the device into IEEE Std 1581 test mode. When this pin is activated, the I/Os of the 1581-compliant device are connected to the test circuitry, instead of its' functional logic. In the case of Transparent Test Mode (TTM), entry/exit test mode is controlled by one of various protocols in conjunction with other test requirements, and a dedicated test pin is not required.

Since an IEEE Std 1581 compliant device can be controlled by the IEEE Std 1149.1 test logic, it can also be controlled by an IEEE Std 1149.7 test infrastructure, where the power management features represent an added-value in relation to the other two test standards.

F. IEEE P1687

IEEE P1687 [14], also known as iJTAG, deals with embedded instrumentation. Complex boards are increasingly populated with high-speed ICs and memories, where the use of test points is no longer feasible. The lack of such test points makes it more difficult to capture structural defects such as opens and shorts, as well as to detect missing / wrong components.

The objective of IEEE P1687 is to offer a method and rules to access embedded instrumentation using the IEEE Std 1149.1 TAP, without needing to define the instruments or their features. The iJTAG initiative provides an extension to the IEEE Std 1149.1 aimed at using the TAP to manage the configuration, operation and collection of data from this embedded instrumentation circuitry.

The IEEE P1687 architecture, also referred as IEEE P1687 *Scan Instrument Access Network*, can open or close scan paths with its Segment Insertion Bit (SIB). The SIB acts as a single external bypass register that is capable of providing or denying access to an embedded instrument. The proposal also includes a *Procedural Description Language* (PDL) that specifies an interface to communicate with the internal embedded instruments and with other blocks within the device, overcoming the limitations of the Serial Vector Format (SVF) [18]when dealing with the SIB registers. This proposal enables test equipment providers to access the embedded instruments in the semiconductor devices for testing purposes. Meanwhile, device manufacturers will be able to regain test coverage with minimal cost impact by integrating this solution into their current test process. The companies that rely on interconnection testing will be the most benefited.

Besides the obvious advantages of using only two pins and dedicated scan formats, the IEEE Std 1149.7 can be adapted to perform almost every IEEE P1687 operations. In fact these standards share a number of similarities, like the chip-level bypass of the IEEE Std 1149.7 and the SIB of the IEEE P1687. There are some portability concerns to take into account, since the IEEE P1687 has its own PDL language. On the other hand, the power management features of IEEE Std 1149.7 are not supported by P1687.

G. IEEE P1838

IEEE P1838 [15] is a proposed standard for the test access architecture of 3D stacked ICs (3D-SICs). The 3D-SIC technology uses Through Silicon Vias (TSVs) to enable die-to-die connections. The number of these devices is increasing due their ability to enable smaller chips with higher signal densities and higher bandwidth, at lower power consumption and cost. The main test challenges are related to test access and to vertical test signal routing. It is also possible that each die has its own test protocol, complicating the test scenario even further. The proposed standard defines a die-level architecture on the basis that compliant dies in the stacked IC will facilitate data transport and test signal routing. Concerning the hardware aspects, the proposal addresses the test signal routing problem, the test interface into the die, and creates die-level wrappers to partition on-die logic and to provide a mechanism for die-to-die communication. It also aims to optimize the protocol and description language for test logic insertion and test generation, and to differentiate pre-, mid-, and post bond test requirements. IEEE P1838 does not assume specific fault/defect models, DfT architectures or test generation methodologies. Wherever applicable it uses the IEEE Std 1149.X for test access ports, the IEEE Std 1500 for on-chip standard DfT architectures, and the IEEE P1687 for design-for-debug architecture.

3D-SICs are increasingly used, and the lack of an appropriate test methodology might prevent access to DfT logic. This standard is die-centric and is not meant to address stack/product-centric challenges, which is where the IEEE Std 1149.7 comes in. The die test infrastructure may be inserted in an IEEE Std 1149.7 architecture to control the whole stack. Since the standard can operate using two pins, the number of TSVs dedicated to D&T are reduced. The star topology is also very useful, since each die may have separate TAPCs. The power management features can also have a positive impact in this type of circuits.

H. Nexus 5001

The NEXUS 5001 standard [16] offers access ports and communication protocols to cope with the challenges faced by debugging infrastructures, with an emphasis in real time applications. Its goal is to create a rich debug feature set, while minimizing pin-count and die area, and ensuring both processor and architecture independency. It can support multi-core and multi-processor designs. This standard defines a set of connectors to enable the communication between the debug tool and the target system, and ensures data transfer using a packet-based protocol. The IEEE Std 1149.1 protocol is used in the case of Class 1 compliant scenarios (there is a total of 4 classes, where Class 4 is the one with more features). NEXUS enables Run-time control, Memory access, Breakpoints, Tracing, and Data acquisition.

In 2009, when the latest NEXUS 5001 revision took place, efforts were made to upgrade the communication protocol to IEEE 1149.7.

V. CONCLUSIONS

All standards that were presented are based on (or depend upon) the IEEE Std 1149.1. Consequently, they all benefit from the improvements introduced by IEEE Std 1149.7. This new test standard is backwards-compatible to 1149.1 and significantly improves the D&T features of new devices, while increasing the performance of all the other standards that have IEEE Std 1149.1 as a predecessor. The IEEE Std 1149.7 key features, such as the two pin TAP, the star topology, one bit bypass and individual addressing, and the power management functions, are vital for a new breed of ICs and their unavoidable D&T challenges.

The use of a 2-pin TAP could provide an advantage when using all other standards that use the IEEE Std 1149.1 communication protocol. The introduction of the star topology may cause a significant impact on the IEEE Stds 1532, 1581 and proposal P1838. The chip-level bypass and individual addressing provided by the IEEE Std 1149.7 are useful in all the standards briefly described and analyzed in this paper, since it provides the means for much more efficient tests. The power management options of this new standard are a key advantage over the IEEE Std P1687, and are very useful on every other standards, especially if they are implemented on mobile battery operated devices that require periodic testing.

We are witnessing an increasing acceptance of this new standard by major industry players, as proven by the recent announcement of Texas Instruments regarding their OMAP ™ 4 platform [19]. Also IEEE std 1149.7 is a recommended test and debug interface according to MIPI, the Mobile Industry Processor Interface Alliance [20].

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