# A VHDL Library for MTM/BST Communication

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## Abstract

The IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture, shortly referred as BST (Boundary Scan Test), specifies a board-level testability infrastructure which was developed in response to ever increasing test challenges posed by high pin-count VLSI integrated circuits and double-side surface -mount printed circuit boards. While presently restricted to structural testing of digital circuits, the BST standard has already been widely accepted at different industry levels. Complex systems will however in most cases consist of several printed circuit boards, which raises the need for a system-level test strategy, presently under development as the IEEE Proposed 1149.5 Standard Test and Maintenance Bus, shortly referred as MTM. The interface between the system-level MTM test bus and the board-level BST test bus has only recently been defined (with the latest draft proposal, from October of 1993), making it possible to develop the necessary protocol conversion blocks. The development of high-level functional models for these blocks, specially if based in a standard representation format, will be useful to every design and test engineer involved in the development of complex systems, since it will enable the reusability of proven models optimising time and risk issues. Moreover, if VHDL models are developed for these blocks, conformance with a large number of automatic synthesis tools will be guaranteed, allowing each new design to use the latest technologies available by simply re-synthesising for the new target technology. This paper describes a library of VHDL models developed to achieve this goal.