Board-Level BIST Based on the 1149.1 Standard

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Abstract

The progress in the fields of miniaturisation (surface mount technology, large pin count ICs, etc.) and integration density (due to feature size reduction, and exploited by the availability of highly sophisticated CAD design tools) has made it possible to design very complex printed circuit boards (PCBs), which present very high testability requirements. Boundary Scan design and test is now largely accepted as one of the most promising solutions for this challenge, with an increasing number of off-the-shelf BST components becoming available, and easy-to-use software tools which automate the development of the boundary scan infrastructure for ASIC design. Board-level test, which was the main driving force behind the development of the BST standard, is however still waiting for an integrated family of components able to address three main requirements: the test of non-BST clusters, analog I/O interface, and board--level BIST capability. Proposed solutions for these problems have been published and some components are available, but a much larger offer for board-level designers is still required.

This paper proposes a board-level BIST strategy based on three types of testability building blocks: the interface to non-BST digital I/O nodes, the interface to analog I/O nodes, and a dedicated test processor providing the board-level test capability. It is shown that, by following careful design rules, it is possible to implement all the proposed building blocks in medium-complexity programmable logic devices (PLDs) widely available, therefore providing a low-cost and maximum-flexibility solution for board-level BIST. Moreover, and since these testability blocks were implemented using a simple and powerful hardware design language (HDL), any changes due to specific board requirements can easily be made.