Course Unit Description - (PHADI)

(Digital Hardware Design)

(Mestrado em Engenharia Electrotécnica e de Computadores)

Academic year: 2009/2010

Subject group: Electrónica e Telecomunicações

	Semestral	**Compulsory**		
Mode of study	Diurno	**Hours / Week**	**T-**Teórica	2
Year	1º		**PL-**Prática-Laboratorial	2
Semester	1º		**OT-**Orientação Tutorial	1

ECTS 6

Objectives

Generic goals:
• The main goal of this course is to explore the fields of digital hardware design, hardware specification languages, computer aid design tools and study and implementation of logic circuits using programmable logic.

Specific goals (Skills):
Intermediary goals
The student should be able of:
• Solving problems requiring the use of digital circuits, developing and presenting a possible solution;
• Studying different tools, languages and development environments;
• Searching on the web, selecting and understanding the meaning of relevant information for the course and the field of digital hardware design.

End-of-course goals
The student should be able of:
• Analysing a given problem requiring the use of logic circuits, formulate the requirements of the solution, describe the circuit, simulate and implement it, using programmable logic devices, and verify it;
• Elaborating a report describing the work done using text and graphic software processing tools;
• Developing integrated solutions and to give its opinion based on solid subject knowledge.

Course Contents

1. Introduction to Digital Hardware Design
1.1. Basic overview of logic functions
1.2. Introduction to hardware description languages
1.3. Introduction to digital hardware design tools
2. Gate-Level Combinational Circuits
2.1. General description
2.2. Structural description
3. Programmable Logic Devices
3.1. Evolution of the programmable logic devices (PLD)
3.2. PLD architectures
3.2.1. Logic blocks architecture
3.2.2. Input/Output blocks architecture
3.2.3. Routing resources architecture
3.3. Programming technologies
4. Logic Design Flow
4.1. Design specification
4.2. Logic simulation
4.3. Synthesis and mapping
4.4. Temporal analysis
5. Regular Sequential Circuit
5.1. Introduction
5.2. HDL code of the FF and register
5.3. Simple design examples
6. Finite State Machines
6.1. Mealy and Moore machines
6.2. FSM representation
6.3. FSMs with data path
7. IP Cores
7.1. Types of cores
7.2. Integration of cores in the user's design
7.3. Customization of cores

Recommended reading

FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 Version. Pong P. Chu, Wiley-Interscience, 2008

Manual de VHDL: Síntesis lógica para PLDs. Javier García Zubía, Universidad de Deusto, 2ª edición, 2005

Teaching Methods

The format will be theoretical and practical. A set of subjects, proposed for autonomous work and presentation during tutorial classes, complements the theoretical classes.
Practical classes take place in a lab environment. The student has to design, simulate and implement small circuits to solve specific problems proposed by the lab teacher.

Assessment methods

• Final lab work and report (60% of the final mark)

The student must do a final lab work consisting of design, simulation and implementation of a circuit whose minimum functionality will be defined by the teacher
The report must be submitted to the teacher to be evaluated before the deadline

• Research and seminars (40% of the final mark)

The student must attend a minimum of 2/3 of the tutorial classes
Tutorial assignments based on research and preparation of seminars about particular subjects of interest to the course

• The reports and seminars are strictly individual and will not be returned to the student

• Lab work and reports, and final exam marks will be round to the nearest tenth. The final mark will be round to the nearest whole number.

	Name
Teacher responsible:	Manuel Gradim de Oliveira Gericota (MGG)
Lecturer:	Manuel Gradim de Oliveira Gericota (MGG)